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p-Channel Oxide Thin Film Transistors Using Solution-Processed Copper Oxide

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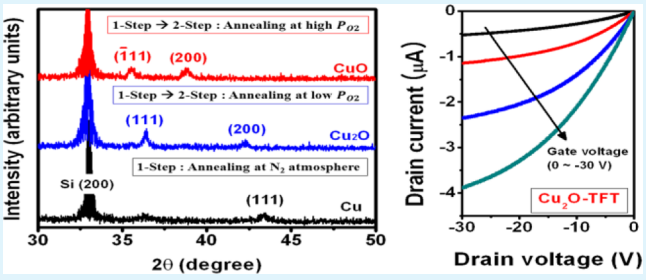
Supporting Information

ABSTRACT: Cu_2O thin films were synthesized on Si (100) substrate with thermally grown 200-nm SiO_2 by sol−gel spin coating method and postannealing under different oxygen partial pressure (0.04, 0.2, and 0.9 Torr). The morphology of Cu_2O thin films was improved through N_2 postannealing before O_2 annealing. Under relatively high oxygen partial pressure of 0.9 Torr, the roughness of synthesized films was increased with the formation of CuO phase. Bottom-gated copper oxide (Cu_xO) thin film transistors (TFTs) were fabricated via conventional photolithography, and the electrical properties of the fabricated TFTs were measured. The resulting Cu_2O TFTs exhibited *p*-channel operation, and field effect mobility of 0.16 $cm^2/(V\ s)$ and on-to-off drain current ratio of $\sim 1 \times 10^2$ were observed in the TFT device annealed at P_{O_2} of 0.04 Torr. This study presented the potential of the solution-based process of the Cu_2O TFT with p-channel characteristics for the first time.



KEYWORDS: *Cu_2O, p-type oxide semiconductor, p-channel TFT, sol−gel, oxidation, two-step annealing, oxygen partial pressure*

1. INTRODUCTION

Oxide-based thin film transistors (TFTs) have received much attention as alternatives to conventional amorphous Si (*a*-Si)-based TFTs because of their superior electrical and optical properties including transparency. The charge transport in the bottom of the conduction band in covalent semiconductors consisting of sp^3 orbital is significantly affected by bond angle, which results in low mobility and instability of *a*-Si TFTs. In contrast, the carrier transport paths in oxide semiconductors are composed of metal *ns* orbitals. The overlap between neighboring metal *ns* orbitals in oxide semiconductors is possible even in an amorphous phase.[1] As a result, oxide semiconductors are relatively insensitive to the presence of structural disorder and high charge carrier mobilities are achievable in amorphous structures. Thus, oxide-based TFTs are very attractive as the driving backplane in active-matrix (AM) organic light-emitting diodes and AM liquid crystal display applications. Until now, many studies on the development of oxide semiconducting materials have focused on n-channel layer fabrication by vacuum processes (ZnO,[2] SnO_2,[3] In_2O_3,[4] ZnInO,[5] InGaO,[6] and InGaZnO[7]) and by solution processes (ZnO,[24,25] In_2O_3, ZTO, IZO,[26] IGZO[27]). In contrast, there have been only a few reports on p-channel TFTs because of lack of naturally *p*-type oxide semiconductors and difficulty in high-quality film growth.[8−10,21,22] The main factors that limit semiconductor properties of p-type oxide are the localized 2*p* orbitals in the valence band maximum (VBM), the deep VBMs (∼5−8 eV) and self-compensation by donors.[23] Although developing p-channel oxide films is challenging, it is necessary for the realization of complementary metal oxide semiconductors and the formation of p−n diodes using all oxide materials.[21]

Cu_2O, SnO, and NiO show representative intrinsic p-type characteristics with enhanced hole conduction.[11−13] Among these oxide materials, Cu_2O has a direct band gap of 2.1 eV[14] and exhibits high hole mobility theoretically exceeding 100 $cm^2/(V\ s)$.[15] Thus, the Cu_2O films are considered as a p-type candidate in p−n junction-based oxide solar cells. Cu_2O-based TFTs have also been studied with high vacuum processes, such as pulsed laser deposition[8] and sputtering.[9,22] However, even with expensive equipment and high-temperature processes, the field effect mobilities of these TFTs are still unsatisfactory.

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Matsuzaki et al. reported low field effect mobility of 0.26 $cm^2/(V\ s)$ using Cu_2O films grown by pulsed laser deposition, despite high hole mobility (~90 $cm^2/(V\ s)$).[8,19] Fortunato et al. produced Cu_2O thin films by thermal treatment at 200 °C for 10 h[9] and fabricated Cu_2O TFTs with field effect mobility of 1.2×10^{-3} $cm^2/(V\ s)$. Recently, Yao et al. reported the room temperature fabrication of p-channel Cu_2O TFTs with superior transfer performance (field effect mobility ~2.40 $cm^2/(V\ s)$ and current on/off ratio ~3.96×10^4) on flexible polyethylene terephthalate substrates.[22] Such low processing temperatures and good electrical performance of the p-type Cu_2O TFTs suggests the potential for fabrication of p-channel Cu_2O layers using solution-processing techniques, such as sol–gel.

Recently, inkjet printing of inorganic materials has received attention for active devices. The importance of solution processing is emphasized in these applications, and TFTs using *n*-type semiconducting oxide fabricated by solution-based processes have been actively reported.[16] On the other hand, there have been only a few reports on the development of solution-based p-type oxide thin films, and their main application has been in photovoltaics. Although Cu_2O thin films synthesized by spin coating method for photovoltaics were reported, they cannot be used in TFT devices due to their poor surface uniformity.[17] In this study, we report on the synthesis of Cu_2O thin films with p-type characteristics by sol–gel spin coating method, and on their performance in TFTs. In particular, we introduce a two-step annealing process for the formation of Cu_2O films and investigate the effect of postannealing process[20] in oxygen atmosphere on the electrical properties of the fabricated Cu_2O TFTs.

2. EXPERIMENTAL DETAILS

Cu_2O thin films were synthesized by a sol–gel spin coating method. Cu (II) acetate hydrate [$Cu(COOCH_3)_2{\cdot}xH_2O$, 98%, Aldrich] was used as a metal cation precursors. A solution was prepared by dissolving 0,7 M of Cu (II) acetate hydrate in 2-methoxyethanol ($CH_3OCH_2CH_2OH$, 99.8%, Aldrich), and 1.4 M of monoethanolamine (C_2H_7NO, 98%, Aldrich) was added to the solution as a stabilizer. The solution was stirred at 60 °C for 1 h and aged for 24 h at room temperature. Si (100) wafer a 200-nm with thermally grown SiO_2 layer was used as the substrate. Before the spin coating process, the substrates were cleaned by sonication in acetone, ethanol, and distilled water for 10 min each, and continuously exposed to 185 nm UV light for 20 min. The UV light treatment is used to improve the surface uniformity. The precursor solution was spin-coated on the substrates at 2000 rpm for 1 min, followed by drying at 150 °C for 20 min on a hot plate. Spin coating and drying were repeated 2 times. Then, the films were annealed at 1.5 Torr with an N_2 (99.999%) flows of 50 sccm at 400 °C for 30 min. After annealing under N_2 atmosphere, the films were annealed under O_2 (99.999%) atmosphere at 700 °C for 30 min under varying oxygen partial pressures of 0.04, 0.2, and 0.9 Torr. During the annealing process, background pressure was kept at 2×10^{-3} Torr and 2, 5, and 10 sccm of oxygen were introduced. The microstructural characterization of synthesized films was performed by X-ray diffraction (XRD) (RIGAKU, D/MAX-2500). Morphological changes of the films caused by variation of oxygen partial pressure were characterized by scanning electron microscopy (SEM) (Philips, XL30S FEG) and transmission electron microscopy (TEM) (JEOL JEM-3010). Cross-sectional TEM samples were thinned mechanically and ion-milled at 3.3 kV using Ar^+ ions. The electrical properties (resistivity and carrier concentration) of copper oxide thin films were characterized by Hall-effect measurement system (Ecopia, HMS-3000).

Bottom-gated TFTs with Cu_2O channels were fabricated by conventional photolithography. Cu_2O films were patterned using an 800 × 1000-μm mask (LxW). In the bottom-gated TFTs fabricated, Si and SiO_2 played the roles of gate and gate dielectric, respectively. The channel width and channel length of the TFTs were 500 and 100 μm, respectively. The source-drain electrodes consist of Ni (30 nm)/Au (70 nm) bilayers formed by e-beam evaporation using a shadow mask after the thermal annealing of channel layers. The electrical properties of the fabricated TFTs were measured using a semiconductor parameter analyzer (Hewlett-Packard, HP 4145B) in a dark room and ambient atmosphere.

3. RESULTS AND DISCUSSION

Figure 1 shows XRD patterns of the copper oxide films synthesized by spin coating method annealed at different

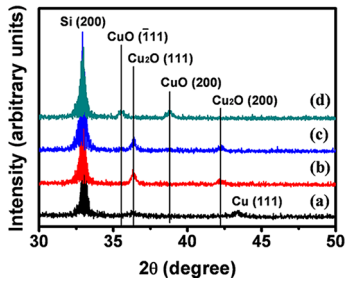

Figure 1. XRD spectra of copper oxide films (a) as-annealed in N_2 atmosphere at 400 °C for 30 min and two-step annealed under different oxygen partial pressures of (b) 0.04, (c) 0.2, and (d) 0.9 Torr.

oxygen partial pressures (P_{O_2}). To investigate the effects of oxygen partial pressure on the electrical properties of resulting films, three oxygen partial pressures were used (0.04, 0.2, and 0.9 Torr). Prior to the annealing in O_2 atmosphere, the sol–gel coated films were first annealed at a fixed temperature of 400 °C in N_2 atmosphere with a working pressure of 1.5 Torr. The XRD results revealed that the film annealed in N_2 atmosphere shows an intense Cu (111) peak (PDF#04–0836) and a very weak Cu_2O (111) peak (PDF#05–0667). This indicates that by annealing in N_2 atmosphere, the sample mainly comprises metallic Cu phase instead of oxide film. Then, additional annealing in O_2 atmosphere transforms the metallic phase into oxidized Cu_2O or CuO films. For the films annealed at 700 °C in O_2 atmosphere with P_{O_2} of 0.04 or 0.2 Torr, similar XRD results were obtained, as shown in spectra b and c in Figure 1. The preparation of oxide films without the first step of annealing in N_2 induces island-shaped film morphology and the formation of nonhomogenous multiphase oxide films. The rough film and the mixed phases consisting of Cu_2O, CuO, and Cu result in low field effect mobility or nonoperation of the oxide TFTs. Therefore, two-step annealing is a very favorable process for TFT fabrication. The detection of intense Cu_2O (111) and weak Cu_2O (200) peaks indicates that Cu phases converted to Cu_2O after annealing in O_2 atmosphere. The Cu-related peaks completely disappeared after O_2 annealing. On the other hand, when annealed at $P_{O_2} \geq 0.9$ Torr, the cupric oxide CuO ($\bar{1}11$) and (200) peaks (PDF#45–0937) were observed, and the peaks of cuprous oxide Cu_2O phase disappeared. These XRD results confirm that the phase of copper oxide can be easily changed depending on the oxygen partial pressure in the second annealing step. Therefore, it is important to precisely control the oxygen partial pressure during the annealing.

Previous reports demonstrated that Cu_2O thin films synthesized by spin coating method grew through a Volmer–Weber island growth mode, instead of layer-by-layer growth

mechanism [19]. However, because the channel thickness is relatively thin and the TFT performance is strongly influenced by film morphology, island-shaped Cu_2O thin film is not suitable for TFT applications. In the Cu_2O thin films with island growth behavior, charge transport can be limited by discontinuous film. This problem was solved by using the two-step annealing process. The spin-coated films were annealed under N_2 atmosphere at 400 °C for 30 min before O_2 annealing. When the Cu_2O thin films are synthesized via Cu phase, the morphology of the film is significantly improved (see Figure S2 in the Supporting Information), compared to the Cu_2O thin film synthesized by single step annealing in O_2 atmosphere (see Figure S1 in the Supporting Information). This emphasizes the importance of the annealing in N_2 atmosphere before oxidation process, despite the formation of metallic phases.

To investigate the film morphology and atomic structure, TEM observations were conducted. Figure 2 shows cross-sectional bright-field TEM images of the synthesized thin films annealed under different P_{O_2} of 0.2 and 0.9 Torr. Like the XRD results, the TEM results also show that phase of the synthesized thin films annealed at P_{O_2} of 0.2 and 0.9 Torr were identified as Cu_2O and CuO, respectively. In the case of the film annealed at P_{O_2} of 0.2 Torr, continuously linked Cu_2O films with larger grain size suitable for TFT applications were observed. The corresponding SADP image reveals that the Cu_2O formed is polycrystalline. In addition, similar film morphology was observed in the sample annealed at P_{O_2} of 0.04 Torr. The thickness of the Cu_2O films annealed at P_{O_2} of 0.04 and 0.2 Torr was ~100 nm. In the case of the CuO thin films, estimation for the absolute film thickness is difficult due to the nonuniform morphologies, as shown in Figure S2 in the Supporting Information. The film annealed at 0.9 Torr showed granular grains with sizes of 60−100 nm, and some voids at the CuO/SiO_2 interface. These voids deteriorate the adhesion of CuO film from SiO_2 substrate. Therefore, when the CuO film is used as a p-channel layer for TFTs, film delamination occurs during the fabrication procedure. These TEM results indicate that the morphology of the copper oxide thin films and quality of interface between the film and substrate were substantially influenced by oxygen partial pressure as well as the phase of the films. At relatively low oxygen partial pressure (0.04−0.2 Torr), continuous films and high-quality interface were fabricated without voids, whereas annealing at 0.9 Torr P_{O_2} formed many voids at the film interface.

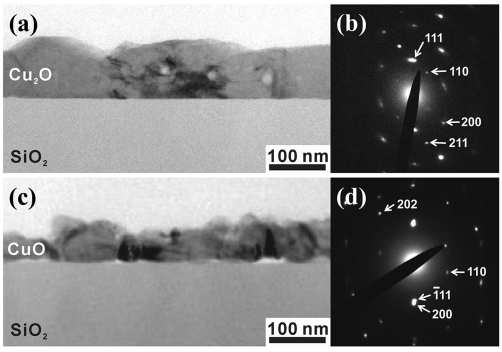

Figure 2. (a, c) Bright-field TEM images and (b, d) selected area diffraction patterns of copper oxide thin films annealed at P_{O_2} of 0.2 and 0.9 Torr, respectively.

Bottom-gate TFTs were fabricated using the Cu_2O and CuO films as channel layers, and the channel width (W) and length (L) were 500 and 100 μm, respectively. Bottom-gated structure was adopted for simple fabrication. The output characteristics of synthesized copper oxide TFTs annealed at P_{O_2} of 0.04, 0.2, and 0.9 Torr are shown in Figure 3a−c, respectively. The drain to source voltage (V_D) is swept from 0 to −30 V, and the gate to source voltage (V_G) is also varied from 0 to −30 V. The output characteristics of the Cu_2O films annealed at P_{O_2} of 0.04 and 0.2 Torr with carrier densities of 1×10^{15} to 1×10^{16} cm^{-3} (obtained from Hall measurements) show that they operate as p-channel TFTs. However, the CuO film annealed at P_{O_2} of 0.9 Torr behaves like an insulator with low driving current. The drain current of the CuO TFT was on the order of 1×10^{-9} A. The interface roughness at the channel/dielectric layer and grain size within channel layer is important for performance of TFT devices. The interface roughness at the channel/dielectric layer and the grain size within the channel layer significantly affect the performance of TFT devices. The rough interface and the small grain size are expected to obstruct the transport of mobile carriers.[29,30] As shown in Figure 2 and Figure S2 in the Supporting Information, the CuO channel has nonuniform morphology with voids at the CuO/SiO_2 interface, and consists of granular grains with small size. Therefore, these results are responsible for the unsatisfactory TFT electrical characteristics.

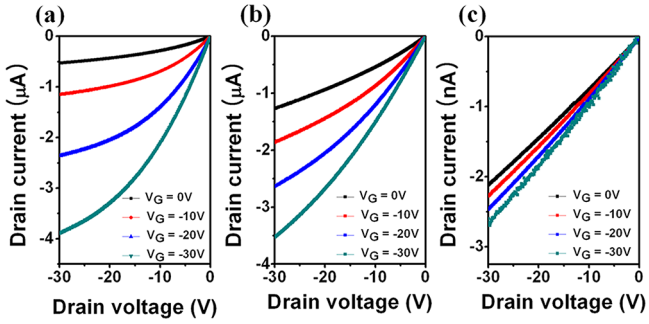

Figure 3. Output characteristics of copper oxide TFTs annealed at P_{O_2} of (a) 0.04, (b) 0.2, and (c) 0.9 Torr. V_D is swept from 0 to −30 V and V_G is varied from 0 to −30 V.

The transfer characteristics and corresponding gate leakage current of the Cu_2O TFTs annealed at P_{O_2} of 0.04 and 0.2 Torr are shown in Figure 4. Both TFT devices annealed at P_{O2} of 0.04 and 0.2 Torr operated in the depletion mode. The currents of the TFTs measured at V_G = 0 V and V_D= −10 V were 1.8×10^{-7} and 6.2×10^{-7} A for the samples annealed at 0.04 and 0.2 Torr, respectively. Also, the maximum current flows at V_D= −10 V were 1.7×10^{-6} and 1.8×10^{-6} A for the samples annealed at 0.04 and 0.2 Torr, respectively. The ratio of $I_{max.}(1.7 \times 10^{-6})/I_{min.}(2.0 \times 10^{-8})$ at V_D= −10 for the TFT annealed at 0.04 was about $\sim 1 \times 10^2$.

The field effect mobility is estimated using the following equation[18]

$$\mu_{FE} = \frac{\partial I_D}{\partial V_G}\frac{L}{WC_iV_D}$$

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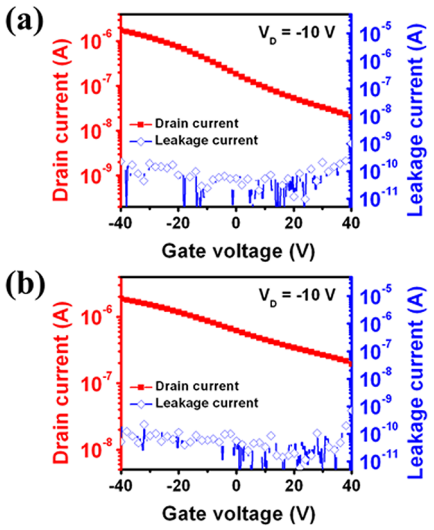

Figure 4. Transfer characteristics as a function of gate voltage for the copper oxide TFTs annealed at P_{O_2} of (a) 0.04 and (b) 0.2 Torr.

where C_i, W, and L are the gate dielectric capacitance per unit area, channel width, and channel length, respectively. The field effect mobility was determined by the maximum transconductance at a drain voltage of 0.1 V. The values of field-effect mobility of the TFTs annealed at 0.04 and 0.9 Torr are 0.159 and 0.043 $cm^2/(V\ s)$, respectively. Recently, Okamura et al.[28] reported that the field-effect mobility in TFTs with a channel of small W/L ratio could be overestimated due to a fringing electric field without an acceptable accuracy of the source/drain electrodes. A small W/L ratio of 5 may induce overestimation up to about 200%. The Hall mobilities obtained for the Cu_2O thin films annealed under 0.04 and 0.2 Torr P_{O_2} conditions were 18.9 and 4.92 $cm^2/(V\ s)$, respectively, which were about 2 orders of magnitude larger than the field effect mobility. The solution-processed Cu_2O thin films consisted of a polycrystalline with nonuniformly dispersed grains, which induces a lower field-effect mobility due to frequent scattering events.[10] The field effect mobility and on-to-off current ratio of the fabricated Cu_2O TFT are low compared to those of n-type oxide TFTs fabricated by solution process. However, this study shows that Cu_2O TFTs can also be fabricated by solution-based method for the first time, and performance can be improved by optimizing process conditions, such as precursor materials, annealing temperature, and annealing method.

4. CONCLUSIONS

Continuous Cu_2O thin films with p-type characteristics were successfully grown on Si (100) substrate with a 200-nm SiO_2 layer thermally grown by sol–gel spin coating and a two-step annealing process to improve surface uniformity. Using an N_2 annealing, Cu-phase thin film was formed and it was oxidized to Cu_2O by O_2 annealing. We investigated the effects of the oxygen partial pressure in the second-step annealing process on the performance of Cu_2O TFTs. The homogeneous Cu_2O films exhibited p-channel TFT behavior, whereas the CuO TFT acted as an insulator. The maximum field effect mobility of the Cu_2O TFT fabricated by solution process was 0.16 $cm^2/(V\ s)$. This research is the first report on the fabrication of the Cu_2O p-channel TFT using a solution process, which will pave the way for the development of solution-based p-channel oxide TFTs.

■ ASSOCIATED CONTENT

Supporting Information

Associated content, including annealing procedure, TEM image, and SEM images. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

‡S.Y.K. and C.H.A. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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